



PATENT ABSTRACTS OF JAPAN

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H01L 29/78**H01L 21/336****H01L 21/8238****H01L 27/092**(21) Application number: **10372194**(71) Applicant: **FUJITSU LTD**(22) Date of filing: **28.12.98**(72) Inventor: **OTA HIROYUKI****(54) SEMICONDUCTOR DEVICE AND
MANUFACTURE THEREOF**

impurity diffusion layer 32a is formed under the side wall insulating film 26a in the silicon substrate 10.

(57) Abstract:

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PROBLEM TO BE SOLVED: To suppress a short channel effect by a method wherein a source/drain diffusion layers are formed on a semiconductor substrate on each side of a gate electrode, a side wall insulating film is formed on the sides of the gate electrode, and an impurity diffusion layer is provided inside the semiconductor substrate under the insulating film.

SOLUTION: An element isolation region 12 is formed on a silicon substrate 10, and an N-type well 14 and a P-type well 16 are each formed on each side of the element isolation region 12. A gate insulating film 18 is formed on the silicon substrate 10 where an N-type well 14 is formed, and a gate electrode 20a and a high-melting metal silicide film 22a are successively formed on the gate insulating film 18. Then, side wall insulating films 26a and 28a are formed on the side of the gate electrode 20a. A low-concentration region 30a and a high-concentration region 30b are formed on each side of the gate electrode 20, and a source/drain diffusion layer 30 is composed of the regions 30a and 30b. An

